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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/026,305	12/18/2001	Timothy D. Thompson	01-849	8081

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EXAMINER	
STOYNOV, STEFAN	
ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/026,305	THOMPSON ET AL.	
	Examiner	Art Unit	
	Stefan Stoynov	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/18/2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 7-22* is/are rejected.

7)☒ Claim(s) *5 and 6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892) •
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Objection to the Abstract

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The first paragraph in the abstract is a repetition of the information given in the title.

Objection to the Title

The disclosure is objected to because of the following informalities:

The title is not placed at the top of the first page of the specification.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "METHOD AND APARATUS FOR TRANSFERRING DATA BETWEEN A SLOWER CLOCK DOMAIN AND A FASTER CLOCK DOMAIN IN WHICH ONE OF THE CLOCK DOMAINS IS BANDWIDTH LIMITED".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-4 and 7-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kincaid and DuLac, and further in view of Nguyen.

Re claim 1, Kincaid discloses a data transfer apparatus for transferring data from a first clock domain to a second clock domain (column 1, lines 27-29), the data transfer apparatus comprising a first bank of registers having an input and an output (FIG. 5, DATA TRANSFER BANK 550), wherein the input receives a first size of data (FIG. 5, 505) and the output outputs a second size of data in which the second size of data is twice the first size of data (FIG. 5, DATA TRANSFER REGISTERS 510); a second bank of registers having an input and an output (FIG. 5, DATA TRANSFER BANK), wherein the input receives a first size of data (FIG. 5, 505) and the output outputs a second size of data in which

the second size of data is twice the first size of data (FIG. 5, DATA TRANSFER REGISTERS 510); and a switch having a first input connected to the output of the first bank of registers, a second input connected to the output of the second bank of registers and an output, wherein the switch selects data from one of the first bank of registers and a second bank of registers for output to the second clock domain (FIG. 5, 511).

Kincaid fails to disclose alternative filling and transferring of data in the registers during the data transfer process.

DuLac teaches a multiple buffer controller (column 1, lines 54-59), wherein filling of data occurs in an alternating fashion between the first bank of registers and the second bank of registers such that one bank of registers is filed with data while another bank of registers transfers data (column 1, lines 66-68 and column 2, lines 1-5) in order to increases the data transfer speed (column 2, lines 6-8). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the alternative filling/transferring of data in the registers, as suggested by DuLac for the data transfer apparatus disclosed by Kincaid.

Kincaid and DuLac fail to disclose transferring the data to a synchronizer unit.

Nguyen teaches a synchronizing mechanism (FIG. 2, synchronizing mechanism 54). In Nguyen, the synchronizing mechanism is part of a synchronizer used for synchronizing data transfer between a first and a second clock domain having different clock signal rates (column 2, lines 1-12). It would

have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the synchronizing mechanism, as suggested by Nguyen for the data transfer apparatus disclosed by Kincaid and DuLac in order to synchronize the data transfer between a first and a second clock domain.

Re claim 2, Nguyen teaches a synchronizer unit (FIG. 2, synchronizing mechanism 54) connected between the first and second clock domain (FIG. 1, CLOCK-SYNC 12).

Re claim 3, Kincaid discloses the data transfer apparatus, wherein the switch is a multiplexer (FIG. 5, 511).

Re claim 4, Kincaid discloses the data transfer apparatus, wherein the first bank of registers stack data of the first size to form data of the second size (FIG. 1 and column 2, lines 63-67).

Re claim 7, Kincaid discloses the data transfer apparatus further comprising at least one more bank of registers having an input and an output, wherein the input receives a first size of data and the output outputs a second size of data in which the second size of data is twice the first size (FIG. 5 and column 5, lines 11-14), wherein the switch includes a third input connected to the output of the third bank of registers (not shown) and wherein filling of data and transferring of data in the first bank of registers, the second bank of registers, and at least one more bank of registers rotates between the first bank of registers, the second bank of registers, and at least one more bank of registers to avoid corruption of data transferred to the second clock domain (FIG. 5 and column 5, lines 14-32).

Re claim 8, Kincaid discloses the data transfer apparatus, wherein the first size of data is 16 bits and the second size of data is 32 bits (column 1, lines 49 and 50).

Re claim 9, Kincaid discloses the data transfer apparatus, wherein the first size of data is 32 bits and the second size of data is 64 bits (FIG. 5).

Re claim 10, Nguyen teaches a data transfer apparatus, wherein the first clock domain is slower than the second clock (column 2, lines 17-21, FIG.1, column 8 lines 49-51, and FIG. 4B).

Re claim 11, Kincaid discloses a method for data transfer between a clock domain having a first bandwidth and a clock domain having a second bandwidth in which the first bandwidth is smaller than the second bandwidth (column 7, lines 3-5, lines 13 and 14). Kincaid further discloses the data being transferred on every clock cycle of the first bus (column 7 lines 6-8) and stacking data into one group, stacking additional data into another group wherein the one group has a size up to the second bandwidth and the another group has the size of the one group (FIG. 5). Kincaid also describes repeating the stacking steps until data transfer is complete (column 3, lines 25-28).

Nguyen teaches a method for data transfer, wherein the first clock domain is slower than the second clock domain (column 2, lines 30-34, column 8, FIG.1, column 8 lines 49-51, and FIG. 4B).

DuLac teaches stacking additional data into another group while transferring the one group to the second clock domain (column 1, lines 66-68 and

column 2, lines 1-5). In DuLac, the simultaneous stacking/transferring of data increases the data transfer speed (column 2, lines 6-8).

Re claim 12, Kincaid discloses the method, wherein the first size of data is 16 bits and the second size of data is 32 bits (column 1, lines 49 and 50).

Re claim 13, Kincaid discloses the method, wherein the stacking steps are performed using data capture unit (FIG. 5, DATA TRANSFER BANK 550 and DATA TRANSFER BANK).

Re claim 14, Kincaid discloses the method, wherein the data capture unit includes a set of registers (FIG. 5, DATA TRANSFER REGISTERS 510).

Re claim 15, Nguyen teaches a method, wherein the data is passed to the second clock domain using a synchronizer circuit (FIG. 2, synchronizer 50). In Nguyen, the synchronizer is used for synchronizing the transfer of data from a first to a second clock domain (column 2, lines 7-12).

Re claim 16, Kincaid discloses the method, wherein the first bandwidth is 16 bits and the second bandwidth is 48 bits (column 1, lines 49 and 50).

Re claim 17, Kincaid discloses an apparatus for data transfer between a clock domain having a first bandwidth and a clock domain having a second bandwidth in which the first bandwidth is smaller than the second bandwidth (column 7, lines 3-5, lines 13 and 14). Kincaid further discloses the data being transferred on every clock cycle of the first bus (column 7 lines 6-8) and first stacking means for stacking data into one group, second stacking means for stacking additional data into another group wherein the one group has a size up to the second bandwidth and the another group has the size of the one group

(FIG. 5). Kincaid also describes repeating means for repeating initiation of the first stacking means and the second stacking means until data transfer is complete (column 3, lines 25-28).

Nguyen teaches an apparatus for data transfer, wherein the first clock domain is slower than the second clock domain (column 2, lines 17-21, column 8, FIG.1, column 8 lines 49-51, and FIG. 4B).

DuLac teaches stacking additional data into another group while transferring the one group to the second clock domain (column 1, lines 66-68 and column 2, lines 1-5). In DuLac, the simultaneous stacking/transferring of data increases the data transfer speed (column 2, lines 6-8).

Re claim 18, Kincaid discloses the apparatus, wherein the first size of data is 16 bits and the second size of data is 32 bits (column 1, lines 49 and 50).

Re claim 19, Kincaid discloses the apparatus, wherein the stacking means are performed using data capture unit (FIG. 5, DATA TRANSFER BANK 550 and DATA TRANSFER BANK).

Re claim 20, Kincaid discloses the apparatus, wherein the data capture unit includes a set of registers (FIG. 5, DATA TRANSFER REGISTERS 510).

Re claim 21, Nguyen teaches an apparatus, wherein the data is passed to the second clock domain using a synchronizer circuit (FIG. 2, synchronizer 50). In Nguyen, the synchronizer is used for synchronizing the transfer of data from a first to a second clock domain (column 2, lines 7-12).

Re claim 22, Kincaid discloses the apparatus, wherein the first bandwidth is 16 bits and the second bandwidth is 48 bits (column 1, lines 49 and 50).

Allowable Subject Matter

Claims 5 and 6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Re claims 5 and 6, the prior art fails to disclose or suggest "wherein data of the first size is received at the second input" of the multiplexers and latches "wherein the input is connected to the output" of the multiplexers, "and the output is connected to the first input" of the multiplexers.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stefan Stoynov whose telephone number is (571) 272-4236. The examiner can normally be reached on 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
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